60-GHz Compact Dual-Mode On-Chip Bandpass Filter Using GaAs Technology

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***Abstract*— A 60-GHz compact dual-mode on-chip bandpass filter (BPF) is presented using gallium arsenide (GaAs) technology. To demonstrate the working mechanism of the proposed BPF, an *LC* equivalent circuit model is conceived and analyzed for further investigation of the transmission poles and zeros. Finally, a prototype of the BPF is fabricated and tested to validate the proposed idea, whose simulated and measured results are in good agreement. The measurements show that it has a center frequency of 58.7 GHz with a bandwidth of 18.4%, and the minimum insertion loss within the passband is 2.42 dB. The chip size, excluding the feedings, is about 0.158 mm × 0.344 mm.**

***Index Terms*— Bandpass filter, GaAs technology, millimeter wave circuits, on-chip devices.**

I. Introduction

MILLIMETER-WAVE bandpass filters (BPFs) have attracted increasing attention recently with the development of the fifth-generation (5G) communications. Especially, the design of on-chip BPFs is more valuable due to the advantage of small physical sizes, but simultaneously is very challenging. Several methods for the on-chip filter design have been presented in recent years using silicon-based [1]–[7] and III/V [8]–[13] technologies. For instance, conductor-backed half-wavelength resonators and coplanar waveguide feedings were utilized to design a millimeter-wave 35-GHz BPF with two transmission zeros (TZs) in [1], where good stopband characteristics at desired frequencies could be realized. However, the passband insertion loss would be also deteriorated, which was larger than 4.5 dB. In [9], parallel coupled lines and open/shorted stubs were employed to construct two 28-GHz BPFs with high selectivity, nevertheless, only coupled lines would be just over quarter wavelength, resulting in very large sizes of the designed BPFs. In [11], an edge-coupled cell was studied by means of the lumped equivalent circuit and then converted to the resonator for the BPF implementation at 23.5 GHz. However, the design step was complicated and the chip size was still large.

Furthermore, some on-chip BPF works were operated at higher frequencies, e.g., 60-GHz band using CMOS process [14]–[16] and GaAs technology [12], [17], [18]. In [12], an E-shaped dual-mode resonator was employed along with a stepped impedance resonator to design a two-pole BPF, whose topology was similar to the edge-coupled cell in [11]. Consequently, the presented resonator occupied a relatively large die area. In [14], a ring resonator structure with a perturbation patch was proposed to construct a 60-GHz dual-mode BPF, whose method was usually used for the BPF design on the printed circuit board. However, the performance was hardly improved and the circumference of the ring resonator was about one guided wavelength, which was very large. In [15] and [16], second-order BPFs were designed with two transmission poles (TPs) in order to obtain broad bandwidth characteristics, but at the expense of the chip sizes.

In our previous works [17], [18], the theory of spoof surface plasmon polaritons was introduced and then applied in the design of on-chip BPFs. In spite of wideband performance, their sizes were still hardly reduced. In this letter, a first-order dual-mode BPF having two TPs within the passband and a TZ at the stopband is presented using GaAs technology. Instead of second-order design, this approach also can generate two resonance modes within the passband of BPF, thus the trade-off between bandwidth and size can be effectively solved. The measurements show that the designed compact BPF possesses a flat frequency response in the passband with low insertion loss.

II. Design of the 60-GHz On-Chip BPF

Fig. 1(a) shows the stack-up of the standard 0.15-μm GaAs pHEMT technology, where two metal layers M1 and M2 with the thicknesses of 2 μm and 1 μm, respectively, are available for circuit design, and their conductivities are both 4×10^7S/m. The relative permittivity of the GaAs and polyimide films are 12.9 and 2.9, respectively, and their thicknesses are 75 μm and 1.8 μm, respectively. A metallic ground is coated beneath the GaAs material. Using this GaAs technology, a compact dual-mode BPF is designed on M1 layer with a square via to the ground, as illustrated in Fig. 1(b).

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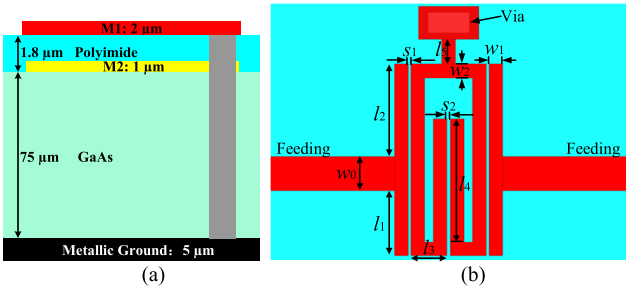

Fig. 1. (a) Stack-up of the employed 0.15-μm GaAs pHEMT technology. (b) Proposed compact dual-mode BPF, where $l_1 = 135$ μm, $l_2 = 95$ μm, $l_3 = 52.5$ μm, $l_4 = 180$ μm, $l_5 = 36$ μm, $w_0 = 50$ μm, $w_1 = 20$ μm, $w_2 = 20$ μm, $s_1 = 4$ μm, and $s_2 = 5$ μm.

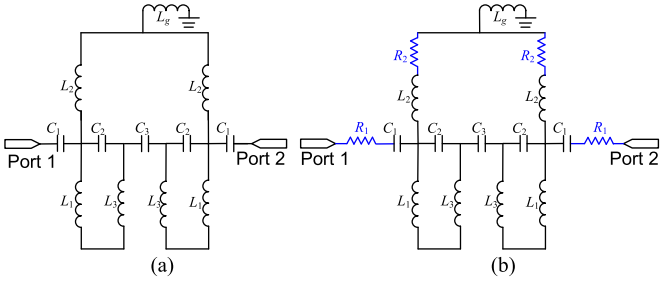

Fig. 2. LC equivalent circuit models of the designed BPF (a) without loss and (b) with loss.

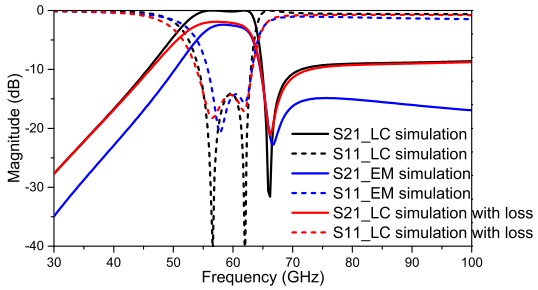

Fig. 3. EM and LC equivalent circuit simulations (with and without loss), where the parameters in Fig. 2 are set as: $L_1 = 111$ pH, $L_2 = 122$ pH, $L_3 = 218$ pH, $L_g = 299$ pH, $C_1 = 12$ fF, $C_2 = 10$ fF, $C_3 = 19.7$ fF, $R_1 = 10.4$ Ω and $R_2 = 0.8$ Ω.

To understand the working mechanism behind the BPF structure, an *LC* equivalent circuit model is constructed in Fig. 2(a). The metal strips coupled to the feeding lines with lengths of (l_1 $+w_0/2$) and (l_2 + $w_0/2$) are assumed as an inductor L_1 and an inductor L_2, respectively. The embedded L-shaped metal strip is represented by an inductors L_3. The gap couplings between the closely spaced metal strips are equivalently demonstrated by five capacitors (i.e., two C_1, two C_2 and a C_3). The short metal strip connected to the square via together with the via itself can be regarded as an inductor L_g, which is short-circuited to the ground. The resistors R_1 and R_2 are inserted as shown in Fig. 2(b) when considering the losses. As demonstrated in Fig. 3, the simulated *S*-parameters of the *LC* equivalent circuits agree reasonably well with the simulations of EM model in Fig. 1(b), where all of them have two TPs (i.e., resonance frequencies) and a TZ. Especially, when the metal and dielectric losses are considered, the insertion loss (IL) of *LC* equivalent circuit in the passband is almost identical to that of the EM model.

To simplify the analysis, the *LC* equivalent circuit model without loss in Fig. 2(a) is used for the odd- and even-mode analysis through bisecting into two halves along the central plane [19], as shown in Fig. 4. For the odd-mode excitation, the central plane in Fig. 2 will behave as a perfect electrical wall and the input impedance of odd-mode equivalent circuit in Fig. 4(a) can be derived as

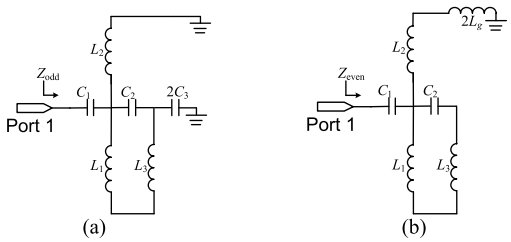

Fig. 4. (a) Odd mode and (b) even mode of the LC equivalent circuit.

TABLE I
PERFORMANCE COMPARISONS WITH SOME PREVIOUS ON-CHIP BPFS

	CFs (GHz)	TZs	Δf (%)	IL (dB)	Size (mm^2)	Size (λ_0^2)	Tech.
[12]	60	2	24.7	1.2	0.232	0.0093	IPD GaAs
[15]	60	3	17	4.1	0.29	0.0115	0.13 μm CMOS
[16]	59.5	1	21.7	3.3	0.054	0.0021	0.18 μm CMOS
[18]	65	0	50.5	1.4	1.175	0.0550	0.15 μm GaAs
This work	**58.7**	**1**	**18.4**	**2.42**	**0.054**	**0.0020 7**	**0.15 μm GaAs**

$$Z_{odd} = j\frac{\omega L_2 - \omega^3 L_4(L_2C_2 + 2L_2C_3)}{2\omega^4 L_2L_4C_2C_3 - \omega^2(L_4C_2 + 2L_4C_3 + 2L_2C_3) + 1} - \frac{j}{\omega C_1}, \quad (1)$$

where $L_4 = L_1 + L_3$. Likewise, when the central plane behaves as a perfect magnetic wall, the half circuit of Fig. 2 will be the even-mode equivalent circuit as seen in Fig. 4(b) and its corresponding even-mode input impedance can be obtained as

$$Z_{even} = \frac{1}{j\omega C_1} + j\omega(L_2 + 2L_g). \quad (2)$$

Therefore, the reflection coefficient S_{11} and transmission coefficient S_{21} of the proposed BPF can be calculated as:

$$S_{11} = \frac{\Gamma_e + \Gamma_o}{2} = \frac{Z_{even}Z_{odd} - Z_0^2}{(Z_{even} + Z_0)(Z_{odd} + Z_0)} \quad (3a)$$

$$S_{21} = \frac{\Gamma_e - \Gamma_o}{2} = \frac{Z_0(Z_{even} - Z_{odd})}{(Z_{even} + Z_0)(Z_{odd} + Z_0)} \quad (3b)$$

The TZ can be determined by setting $S_{21} = 0$, and consequently the condition of $Z_{even} = Z_{odd}$ needs to be satisfied according to (3b). Through calculating (1) equal to (2), the position of TZ is found, which is mainly determined by the capacitor C_3 and inductor L_2. As illustrated in Fig. 5(a), when the value of C_3 increases from 18.7 fF to 20.7 fF, the TZ will be adjusted from 68 GHz to 64.4 GHz, thus the bandwidth of BPF will be decreased accordingly. Similarly, the inductor L_2 can also control the position of TZ, as shown in Fig. 5(b). By setting $S_{11} = 0$ through equation (3a), the two transmission poles can be obtained, one of which on the right side will be also moved as the TZ is adjusted by changing the value of C_3 or L_2. While the other transmission pole on the left side remains fixed. On the other hand, the transmission pole on the left side is mainly determined by the parameters C_1 and L_g, while the one on the right side and the TZ will both keep fixed, as seen in Figs. 5(c) and 5(d).

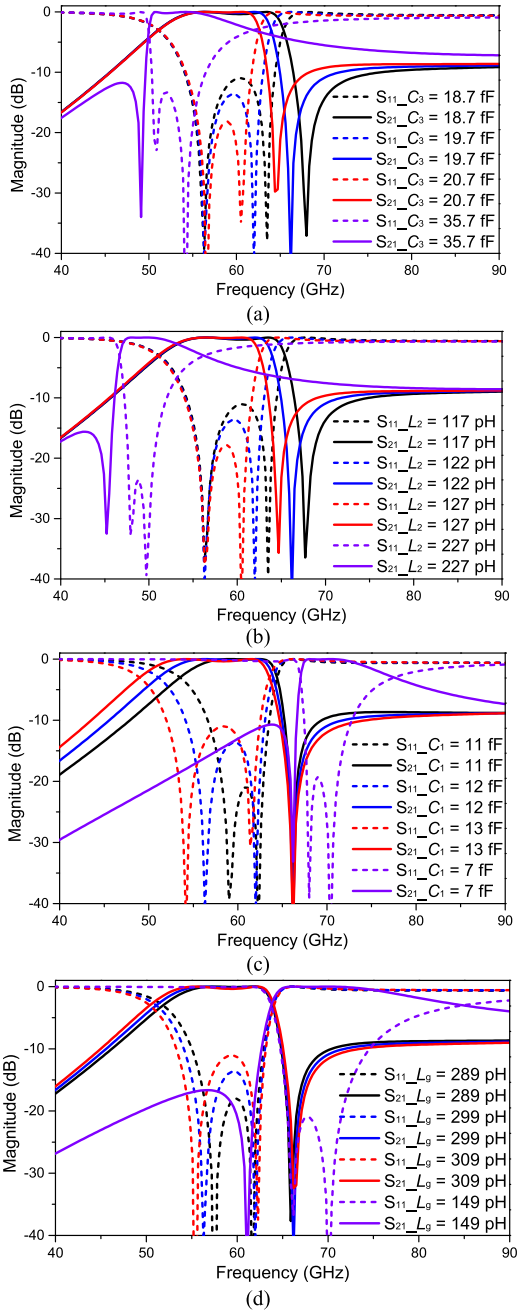

Fig. 5. Simulated *S*-parameters with different values of (a) C_3, (b) L_2, (c) C_1, and (d) L_g.

Moreover, as the value of C_3 (or L_2) further increases to 35.7 fF (or 227 pH), the TZ at the right edge of the passband will be moved to the left edge as seen in Figs. 5(a) and 5(b). Similarly, the TZ can be also moved from the right to left edge of the passband by tuning C_1 or L_g as shown in Figs. 5(c) and 5(d). Therefore, good selectivity of the proposed BPF at the right or left edge of the passband can be easily chosen. Note that the operating frequency of the BPF will be shifted when the TZ is moved from the right edge to the left edge of the passband. But we can adjust the values of C_1 and C_3 to move the operating frequency back to the previous one, i.e., 60 GHz, as shown in Fig. 6(a). Similarly, the values of L_2 and L_g are also tuned to manipulate the operating frequency of the BPF, as demonstrated in Fig. 6(b).

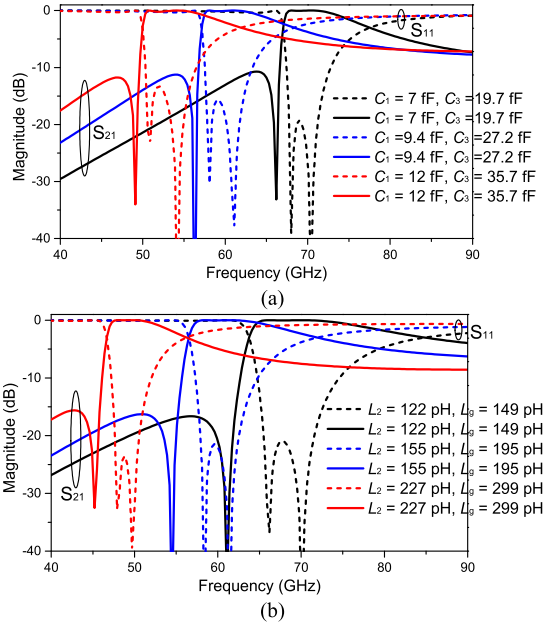

Fig. 6. Adjustment of operating frequency with different values of (a) C_1 & C_3 and (b) L_2 & L_g.

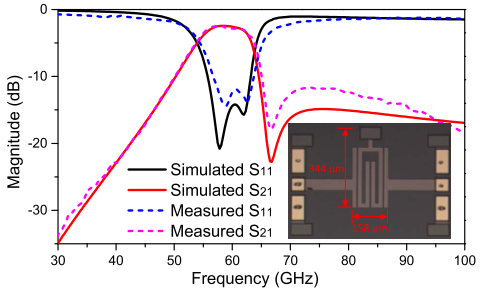

Fig. 7. Simulated and measured results of the proposed BPF.

III. On-Wafer Measurements

For further demonstration of the proposed BPF, an example is fabricated and then measured via an on-wafer ground-signal-ground probing using a vector network analyzer. Fig. 7 shows the EM simulated and measured results of *S*-parameters of the BPF, which are reasonably in good agreement. The measurements show that it has a center frequency at 58.7 GHz with a 3-dB bandwidth from 53.3 GHz to 64.1 GHz (18.4%). The ILs are at the range between 2.42 and 3.07 dB within the passband, and the return losses are better than 12.6 dB. The calculated unloaded quality factor [20] of the proposed BPF is 52, which is higher than the ones in previous works [4], [15], [16].

The die photograph of the designed filter can be seen in the inset of Fig. 7. The chip size, excluding the feedings, is 0.158 mm × 0.344 mm. The performance comparisons with some recently reported on-chip BPFs have been tabulated in Table I. As can be seen, the proposed BPF has the advantages of low IL and small chip size.

IV. Conclusion

A compact GaAs-based dual-mode BPF operating at 60-GHz band has been presented with a simple design topology. Due to its very compact size, low in-band IL and moderate bandwidth, the proposed BPF is readily used for 5G or even beyond 5G communication systems.

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