A Wideband Filtering Switch: Its Synthesis and Design

Kai-Da Xu, *Senior Member, IEEE*, Xiaoyu Weng, Qiang Chen, *Senior Member, IEEE*, and Haijun Fan, *Member, IEEE*

***Abstract*— This article presents a direct synthesis method for the design of a wideband filtering switch, where p-i-n diodes are incorporated into each resonator. As parasitic parameters are embedded in the p-i-n diodes, an ideal transformer is introduced in each resonator to provide the freedom to designate the proper values for inductances and capacitances in the resonators. According to the rejection specification in the ON state, an *N*th order bandpass filter (BPF) network with *N* transmission zeros (TZs) is synthesized, followed by a new circuit model extraction procedure to extract lumped circuits in the BPF network. To simplify the network topology, two ideal transformers at input–output port remain after absorbing the ideal transformers between resonators. Then, the lumped circuit model is converted into a distributed circuit model in the synthesis process, maintaining the filtering response in a wide frequency range when the switch is in the ON state. Besides, the *N* TZs of the filtering switch in the OFF state can be introduced and arranged to suitable positions. Consequently, high isolation within the stopband of the switch in the OFF state can be achieved. For demonstration purposes, two filtering switches with fractional bandwidths (FBWs) of 30% and 50% are fabricated and measured. Good agreement can be observed between the simulated and measured results, which validates the feasibility of the proposed method.**

***Index Terms*— p-i-n diode, single-pole-single-throw (SPST), transmission zeros (TZs), wideband response.**

I. Introduction

AS ONE of the essential components in modern wireless communication systems, microwave switches are utilized to switch the communication channel and control the signal pathway. Due to the poor selectivity of the switch, a filter is usually required in front of it to pass through the useful signal and suppress the interference. In recent years, the co-design of switches and filters has attracted much more attention compared with conventional independent components since the filtering switch structure has the advantages of improved ON-state selectivity, high OFF-state suppression, low loss of interconnections, and compact size.

To obtain high-performance filtering switches, the devices with inherent switching characteristics are widely utilized to design different switches, such as field-effect transistors (FETs) [1], [2], [3], [4], [5], [6], [7], [8], [9] and p-i-n diodes [10], [11], [12], [13], [14], [15], [16], [17]. Due to the negligible dc power consumption and the ease of integration to amplifiers, FET is mostly used to design monolithic microwave integrated circuit (MMIC) switches. In [1], a single-pole-double-throw (SPDT) switch was reported based on a composite resonator, which consists of a transmission line (TL) and an FET in series. When the FETs are biased below the pinch-off voltage, the frequency response of the switch in the ON state can be designed with filter synthesis methods. In [2], an FET-based resonator was proposed by combining the shorted TL with FET in parallel. By selecting appropriate coupling parameters, the MMIC switches can be easily designed based on the coupled resonator theory. In [5], a filtering switch was presented by replacing the capacitances in the lumped bandpass filter (BPF) with OFF-state transistors. Besides, the FET can be utilized to provide the coupling between adjacent resonators [6] and control ON-state and OFF-state modes of resonators [8].

Similarly, the p-i-n diode is another option with two inherent states based on different bias voltages. The characteristics of p-i-n diode could be used to design switches with several technologies, such as dielectric resonator [10], coaxial cavity [11], low-temperature cofired ceramic (LTCC) [12], and printed circuit board (PCB) [13], [14], [15], [16], [17]. In [10], two p-i-n diodes were connected to two output feedlines, where the switching between two channels was achieved by controlling the coupling between the output feedlines and the dielectric resonator. In [13], the stepped-impedance resonators with p-i-n diodes loaded at one end were used to construct SPDT filtering switches. Excellent isolation in the OFF state could be obtained by properly adjusting the stepped length ratio of the stepped-impedance resonator. In [15], switches consisting of two distributed coupled tri-mode resonators loaded with opposite-polarity p-i-n diodes were presented, where the out-of-band rejection could be improved with the absorptive OFF-state property.

It is noted that most filtering switches integrated with FETs and p-i-n diodes are analyzed and designed by the coupled resonator theory, where the coupling matrix synthesis method is employed. The dimensions of coupling structures

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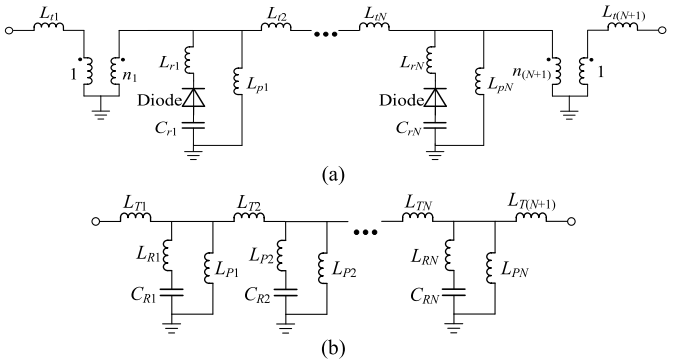

Fig. 1. (a) Proposed wideband filtering SPST switch. (b) Wideband BPF in [18].

could be determined by the coupling matrix generated from the specifications of the switch in the ON state. However, it is challenging to design a wideband filtering switch using the coupling matrix synthesis method due to its narrowband nature. In addition, the characteristics of switches in the OFF state are hardly exploited in the existing synthesis process.

In this article, therefore, a direct synthesis method for the design of a wideband filtering switch has been proposed. A wideband filtering switch with N transmission zeros (TZs) is attained by embedding a p-i-n diode into each resonator and incorporating the p-i-n diode parasitic parameters into the wideband filter synthesis. High isolation within the switch stopband in the OFF state can be achieved by arranging the N TZs in the OFF state properly when converting the lumped circuit model into a distributed circuit model. For demonstration, two filtering switches with fractional bandwidths (FBWs) of 30% and 50% are designed and measured, validating the feasibility of the proposed method.

II. Analysis of Wideband Filtering Switch Embedded With p-i-n Diodes

The proposed wideband filtering single-pole-single-throw (SPST) switch structure is shown in Fig. 1(a), which consists of lumped inductors, capacitors, p-i-n diodes, and two ideal transformers at the input and output ports. Different from the BPF topology in [18], as shown in Fig. 1(b), p-i-n diodes are embedded into each resonator to perform the switch function, and two ideal transformers are introduced at the input and output ports which stem from the synthesis process of the switch ON and OFF states and will be presented later in Section III. Due to parasitic parameters embedded in the p-i-n diodes, an ideal transformer will be introduced in each resonator to provide the freedom to designate the proper values for inductances and capacitances in the resonators. Two ideal transformers at the input and output ports remain after absorbing the ideal transformers between resonators. To simplify the synthesis process, the equivalent circuits of the p-i-n diode under reverse bias and forward bias conditions given in Fig. 2 are adopted [19], [20]. Since R_p in reverse bias is very large (usually in kΩ) and R_0 in forward bias is very small (about or less than 1 Ω), they can be seen as open-circuited and short-circuited, respectively. For convenience, they will both be ignored in the following analysis.

Fig. 3 shows the equivalent circuits of resonator i with p-i-n diode under forward bias and reverse bias, where L_{ri}, C_{ri}, and L_{pi} denote the circuit elements of resonator i. Under reverse bias, whose circuit model is shown in Fig. 3(a), the

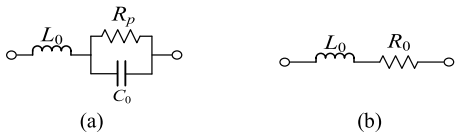

Fig. 2. Equivalent circuits of the p-i-n diode under conditions of (a) reverse bias and (b) forward bias.

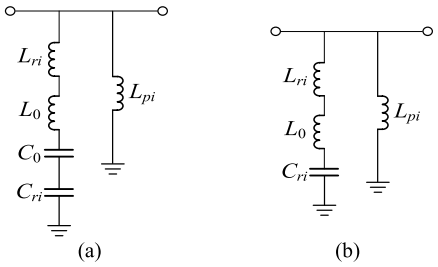

Fig. 3. Equivalent circuits of the resonator in the proposed switch with p-i-n diode under two different biases. Resonator with p-i-n diode under (a) reverse bias and (b) forward bias.

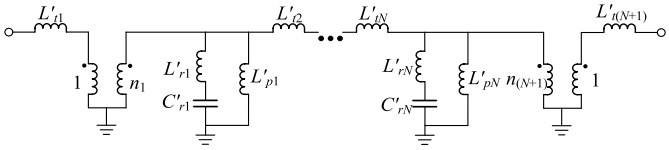

Fig. 4. Wideband BPF network with two ideal transformers.

transmission pole (TP) f_{p_R} and TZ f_{z_R} of the resonator can be found as

$$f_{p\_R} = \frac{1}{2\pi}\sqrt{\frac{C_{ri}+C_0}{C_{ri}C_0(L_{ri}+L_0+L_{pi})}} \tag{1a}$$

$$f_{z\_R} = \frac{1}{2\pi}\sqrt{\frac{C_{ri}+C_0}{C_{ri}C_0(L_{ri}+L_0)}}. \tag{1b}$$

Under forward bias in Fig. 3(b), the TP f_{p_F} and TZ f_{z_F} can be expressed as

$$f_{p\_F} = \frac{1}{2\pi}\sqrt{\frac{1}{C_{ri}(L_{ri}+L_0+L_{pi})}} \tag{2a}$$

$$f_{z\_F} = \frac{1}{2\pi}\sqrt{\frac{1}{C_{ri}(L_{ri}+L_0)}}. \tag{2b}$$

It is noted that $f_{p\_F} < f_{p\_R}$ and $f_{z\_F} < f_{z\_R}$, which means the response of resonator i will shift toward lower frequency under forward bias. Moreover, since $f_{p\_F} < f_{z\_F}$ and $f_{p\_R} < f_{z\_R}$, the TZ of resonator i under both states will be located on the right side of TP. Thus, f_{z_F} in each resonator is to be arranged in the interested frequency band, and no TP under forward bias is in the interested frequency band. This feature gives the feasibility of realizing the filtering switch function and featuring high isolation in the OFF state with such a resonator under forward bias. When the p-i-n diodes are under reverse bias condition, the filtering switch is in the ON state, while with forward bias, it is in the OFF state.

By replacing p-i-n diodes with the equivalent circuit under reverse bias, the filtering switch shown in Fig. 1(a) in the ON state can be transformed into a BPF network, as illustrated in Fig. 4. The BPF network with two ideal transformers can then

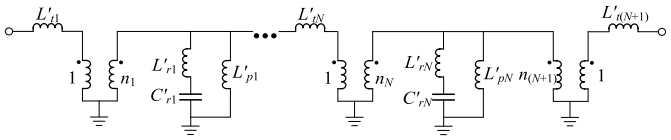

Fig. 5. Proposed Nth order BPF network with $(N+1)$ ideal transformers.

be synthesized and extracted based on the given specifications of filtering switch in the ON state. Next, the circuit elements L_{ri}, C_{ri}, L_{ti}, and L_{pi} of the filtering switch in Fig. 1(a) can be determined by circuit elements L'_{ri}, C'_{ri}, L'_{ti}, and L'_{pi} in Fig. 4. Therefore, the circuit elements of the filtering switch can be calculated by

$$L_{ri} = L'_{ri} - L_0,\ \ C_{ri} = \frac{C_0 C'_{ri}}{C_0 - C'_{ri}},\ \ L_{pi} = L'_{pi} (i = 1, 2, 3, \ldots, N)$$
$$L_{ti} = L'_{ti} (i = 1, 2, 3, \ldots, N, N+1) \tag{3}$$

where L_0 and C_0 are parameters of p-i-n diode under reverse bias. To ensure L_{ri}, C_{ri} is greater than zero, $L'_{ri} > L_0$, and $0 < C'_{ri} \leq C_0$ should be taken into consideration while extracting the circuit model of the BPF network.

III. Circuit Model Extraction

With the given specifications of the filtering switch in the ON state, the filtering function can be synthesized straightforwardly by the process presented in [21]. Based on the filtering function, the overall *ABCD* matrix can be derived [22], from which the circuit elements of the BPF topology can be sequentially extracted. Finally, the elements of the SPST switch are calculated based on (3), which are associated with the parameters of the p-i-n diode under reverse bias. In this work, the extraction process of an Nth-order BPF network with $(N+1)$ ideal transformers given in Fig. 5 is proposed. By introducing an ideal transformer with transforming ratio n_i, L'_{ri}, and C'_{ri} can be designated with proper values meeting the requirements of $L'_{ri} > L_0$ and $0 < C'_{ri} \leq C_0$. Then, the BPF with two ideal transformers in Fig. 4 can be obtained by absorbing the ideal transformers with numbers 2 to N.

As illustrated in Fig. 6, the proposed circuit model extraction procedure for the circuit in Fig. 5 consists of five basic operations: 1) extract a series inductor L'_{ti}; 2) extract an ideal transformer; 3) extract a shunt branch of series L'_{ri} and C'_{ri}; 4) extract a shunt inductor L'_{pi}; and 5) extract the remainder circuit with a shunt inductor, an ideal transformer, and a series inductor. Compared with the extraction method in [18], an additional ideal transformer is extracted between series inductor L'_{ti} and the shunt branch of series L'_{ri} and C'_{ri}, i.e., operation 2) illustrated in Fig. 6(b). Besides, each shunt resonator of series L'_{ri} and C'_{ri} is responsible for the generation of a finite TZ in the ON state. Therefore, the TZs of BPF should be allocated to all resonators before the extraction procedure. Starting from the left-hand side of the network, elements in Fig. 5 will be extracted in sequence. The following equations can present the network transformation during the extraction operations 1)–4) accordingly:

$$\frac{1}{P_1}\begin{bmatrix} A_{n1} & B_{n1} \\ C_{n1} & D_{n1} \end{bmatrix} = \frac{1}{P_2}\begin{bmatrix} A_{n2} + sL'_{ti}C_{n2} & B_{n2} + sL'_{ti}D_{n2} \\ C_{n2} & D_{n2} \end{bmatrix} \tag{4}$$

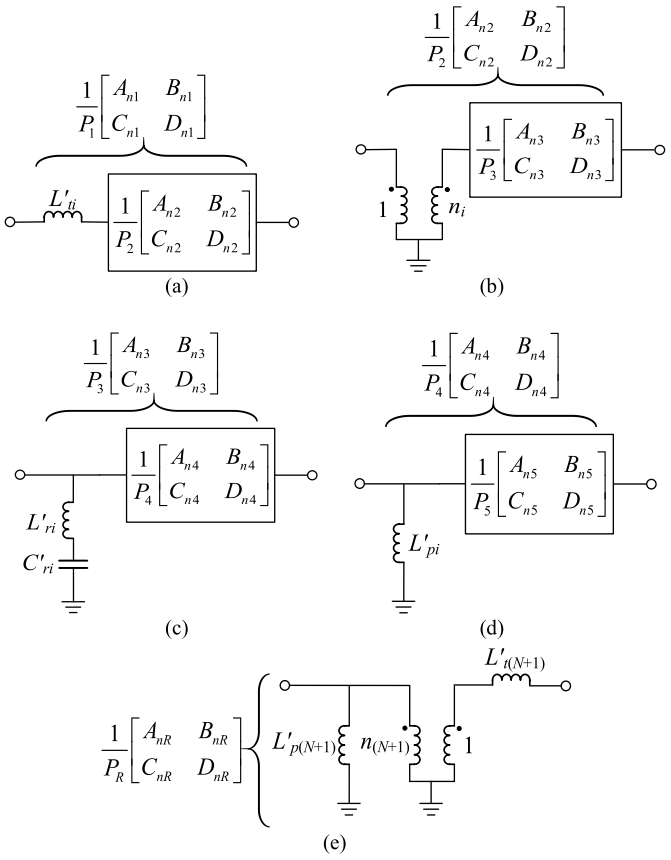

Fig. 6. Five basic extraction operations. (a) Extract a series inductor. (b) Extract an ideal transformer. (c) Extract a shunt branch of series *LC*. (d) Extract a shunt inductor. (e) Extract the remainder circuit with a shunt inductor, an ideal transformer, and a series inductor.

$$\frac{1}{P_2}\begin{bmatrix} A_{n2} & B_{n2} \\ C_{n2} & D_{n2} \end{bmatrix} = \frac{1}{P_3}\begin{bmatrix} \frac{1}{n_i}A_{n3} & \frac{1}{n_i}B_{n3} \\ n_i C_{n3} & n_i D_{n3} \end{bmatrix} \tag{5}$$

$$\frac{1}{P_3}\begin{bmatrix} A_{n3} & B_{n3} \\ C_{n3} & D_{n3} \end{bmatrix} = \frac{1}{P_4(s^2 - s_{zi}^2)} \times \begin{bmatrix} A_{n4}(s^2 - s_{zi}^2) & B_{n4}(s^2 - s_{zi}^2) \\ \frac{1}{L'_{ri}}sA_{n4} + C_{n4}(s^2 - s_{zi}^2) & \frac{1}{L'_{ri}}sB_{n4} + D_{n4}(s^2 - s_{zi}^2) \end{bmatrix} \tag{6}$$

$$\frac{1}{P_4}\begin{bmatrix} A_{n4} & B_{n4} \\ C_{n4} & D_{n4} \end{bmatrix} = \frac{1}{P_5}\begin{bmatrix} A_{n5} & B_{n5} \\ \frac{1}{sL'_{pi}}A_{n5} + C_{n5} & \frac{1}{sL'_{pi}}B_{n5} + D_{n5} \end{bmatrix} \tag{7}$$

where the subscript n denotes the numerator polynomials, e.g., A_{n1} is the numerator polynomial of A_1. s_{zi} is the TZ assigned to the series L'_{ri} and C'_{ri} resonator circuit in the s-plane.

The relationship between denominator polynomials of these *ABCD* matrices (P_1–P_5) can be expressed as

$$P_1 = P_2 = P_3 = P_4(s^2 - s_{zi}^2), \quad P_4 = P_5. \tag{8}$$

Based on (4), the series element L'_{ti} extracted in operation 1) can be calculated by

$$L'_{ti} = \left.\frac{A_{n1} - A_{n2}}{s_{zi}C_{n2}}\right|_{s=s_{zi}} = \left.\frac{A_{n1}}{s_{zi}C_{n1}}\right|_{s=s_{zi}} \tag{9}$$

where $C_{n2} = C_{n1}$ and $A_{n2}(s_{zi}) = A_{n3}(s_{zi})/n_i = A_{n4}(s_{zi})(s_{zi}^2 - s_{zi}^2)/n_i = 0$.

Then, before the extraction of the ideal transformer in operation 2), L'_{ri} should be designated under the constraint of $L'_{ri} > L_0$. Correspondingly, C'_{ri} is in terms of L'_{ri} based on the assigned TZ s_{zi}

$$C'_{ri} = -\frac{1}{s_{zi}^2 L'_{ri}}. \tag{10}$$

Obviously, $0 < C'_{ri} \le C_0$ should be satisfied as well.

From (5) and (6), A_{n2} and C_{n2} can be expressed as

$$A_{n2} = \frac{1}{n_i}A_{n3} = \frac{1}{n_i}\left(s^2 - s_{zi}^2\right)A_{n4} \tag{11a}$$

$$C_{n2} = n_i C_{n3} = n_i\left(\frac{1}{L'_{ri}}sA_{n4} + \left(s^2 - s_{zi}^2\right)C_{n4}\right) \tag{11b}$$

by equaling s to s_{zi}, the transforming ratio n_i can be derived

$$n_i = \left.\frac{C_{n2}}{\frac{1}{L'_{ri}}sA_{n4}}\right|_{s=s_{zi}} = \sqrt{\left.\frac{C_{n2}\left(s^2 - s_{zi}^2\right)}{\frac{1}{L'_{ri}}sA_{n2}}\right|_{s=s_{zi}}}. \tag{12}$$

Through (7), it seems that the shunt inductor L'_{pi} can be determined by

$$L'_{pi} = \frac{A_{n5}}{s(C_{n4} - C_{n5})} = \frac{A_{n4}}{s(C_{n4} - C_{n5})}. \tag{13}$$

However, it is unable to calculate L'_{pi} by eliminating C_{n5} at s_{zi} as the method in (9). To continue the extraction procedure, L'_{pi} should be predefined with an initial value, making all the extracted circuit elements positive. After operation 4), the *ABCD* matrix with the subscript $n5$ can be obtained based on (7), which will be used in the next cycle of extraction operations 1)–4). In the above analysis, the elements are derived from numerator polynomials of A and C at each extraction stage. The same value can be extracted from B and D.

For operation 5), the overall *ABCD* matrix of remainder elements is given by

$$\frac{1}{P_R}\begin{bmatrix} A_{nR} & B_{nR} \\ C_{nR} & D_{nR} \end{bmatrix} = \begin{bmatrix} n_{(N+1)} & n_{(N+1)}sL'_{t(N+1)} \\ \frac{n_{(N+1)}}{sL'_{p(N+1)}} & n_{(N+1)}\frac{L'_{t(N+1)}}{L'_{p(N+1)}} + \frac{1}{n_{(N+1)}} \end{bmatrix}. \tag{14}$$

Therefore, these circuit elements can be obtained

$$L'_{p(N+1)} = \frac{A_{nR}}{sC_{nR}}, n_{(N+1)} = \frac{A_{nR}}{P_R}, L'_{t(N+1)} = \frac{B_{nR}}{sA_{nR}}. \tag{15}$$

Here, $L'_{p(N+1)}$ can be absorbed by the shunt inductor L'_{pN} extracted in operation 4) in the final cycle.

By repeating the basic operations 1)–4) for N times, the circuit elements with numbers 1–N of the proposed BPF in Fig. 5 can be obtained. Then, the remainder elements $L'_{t(N+1)}$ and $n_{(N+1)}$ are extracted by operation 5) to complete the extraction procedure. However, it is difficult to realize the circuits with ideal transformers. Additional circuit transformations should be used to eliminate the ideal transformers. As shown in Fig. 7, the combination of a series inductor and an ideal transformer

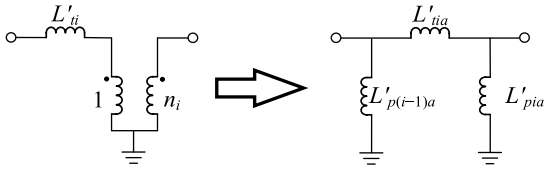

Fig. 7. Transformation of a series inductor cascaded with an ideal transformer.

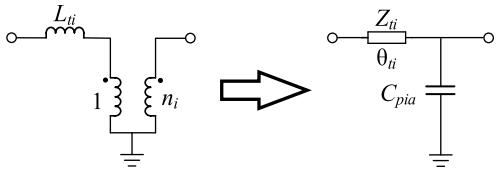

Fig. 8. Equivalent distributed circuit of the network at I/O ports of the switch.

can be replaced by a Π-network of inductors. Equating the *ABCD* matrices of two circuits, the elements of the Π-network can be obtained as

$$L'_{tia} = n_i L'_{ti}, L'_{p(i-1)a} = \frac{L'_{tia}}{n_i - 1}, \quad L'_{pa} = \frac{n_i L'_{tia}}{1 - n_i} \tag{16}$$

where $L'_{p(i-1)a}$ and L'_{pa} have opposite signs. For the ideal interresonator transformers ($i = 2,\ldots, N$), shunt inductors $L'_{p(i-1)a}$ and L'_{pia} of the equivalent Π-network can be absorbed by the adjacent inductors $L'_{p(i-1)}$ and L'_{pi}.

After eliminating the interresonator ideal transformers of the BPF network in Fig. 5, the BPF with two ideal transformers given in Fig. 4 can be obtained, where the values of L'_{pi} ($i = 1, 2,\ldots, N$) and L'_{ti} ($i = 2,\ldots, N$) will be updated due to the absorption of ideal transformers. Besides, the final values of L'_{pi} and L'_{ti} in Fig. 4 will remain unchanged if choosing different initial values of L'_{pi} in operation 4). Only the values of C'_{ri} (L'_{ri}) and the assignment of TZs in the ON state for each resonator will influence the extracted results in Fig. 4. Therefore, different from the extraction method in [18], C'_{ri} (L'_{ri}) is the design freedom of the proposed extraction process, which makes it possible to choose the proper values of C'_{ri} (L'_{ri}) directly. In addition, C'_{ri} and L'_{ri} are also associated with the TZs arrangement in the OFF state, which will be discussed in Section IV-B.

Then, the proposed filtering switch can be obtained by adding a p-i-n diode into each resonator, as shown in Fig. 1(a). The circuit elements of the filtering switch can be determined according to (3). For two ideal transformers located at the input and output ports, they can be eliminated during the approximation of distributed circuits, which will be analyzed in Section IV.

IV. Distributed Circuits Approximations

To implement the filtering switch by distributed circuit, approximations for lumped elements should be introduced under wideband conditions. In addition to the distributed circuit of approximations for L_{ti} ($i = 2, 3,\ldots, N$) readily available in [18], two new distributed approximation circuits, i.e., the I/O coupling network and the resonant circuit with p-i-n diode, are introduced here.

A. Approximation of I/O Coupling Network

To eliminate two ideal transformers at the input and output ports, the network at input–output port as shown in Fig. 8 can

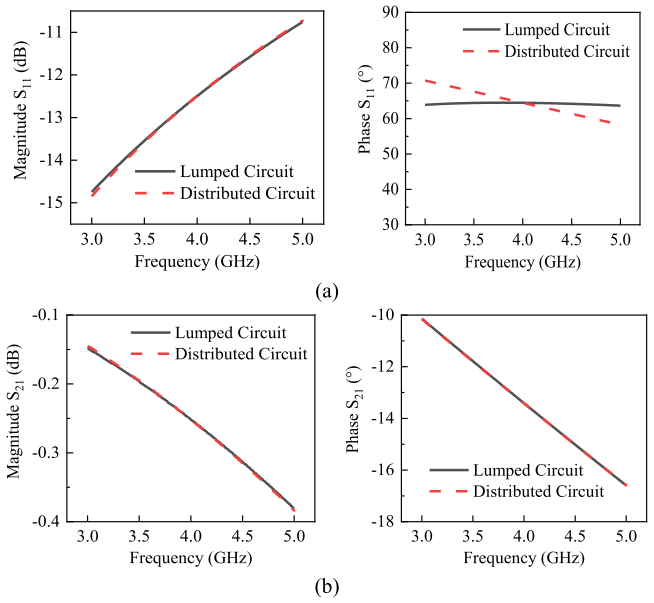

Fig. 9. Frequency responses of lumped element I/O coupling network and distributed element circuit. (a) $S11$ and (b) $S21$.

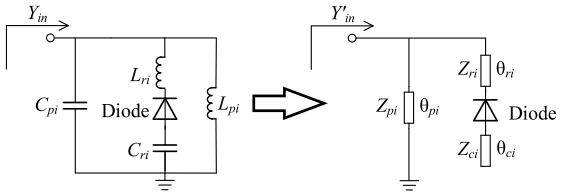

Fig. 10. Approximation of lumped circuit loaded by a p-i-n diode.

be approximated by a TL (Z_{ti}, θ_{ti}) and a shunt capacitor C_{pia}. By evaluating the *ABCD* matrix of the two circuits at the center frequency f_0, the equations can be obtained as

$$\theta_{ti} = \arccos(n_i), \quad Z_{ti} = \frac{\omega_0 L_{ti}}{\tan(\theta_{ti})}, \quad C_{pia} = -\frac{\sin(2\theta_{ti})}{2n_i^2 \omega_0 Z_{ti}} \tag{17}$$

where n_i is less than 1 to ensure θ_{ti} rational. It can be achieved by assigning L'_{ri} and C'_{ri} properly in the extraction procedure of the BPF network. Besides, θ_{ti} is less than $\pi/2$ because the transforming ratio n_i is positive, as seen in (12). Obviously, the capacitance C_{pia} is always negative, which could be eliminated through the approximations of the resonant circuits.

When $f_0 = 4$ GHz, $L_{ti} = 1$ nH, and $n_i = 0.95$, Z_{ti}, θ_{ti}, and C_{pia} are calculated as 76.5 Ω, 18.2°, and −0.171 pF, respectively. The *S*-parameters of these two networks are compared and shown in Fig. 9.

B. Approximation of Resonant Circuit

As illustrated in Fig. 10, the lumped resonant circuit is approximated by a short-circuited stub in parallel with a branch, which is a series of a TL, a p-i-n diode, and an open-circuited stub. To eliminate the negative capacitors generated from approximations of interresonator coupling inductors [18] and I/O coupling networks in (17), a shunt capacitor C_{pi} is included in the approximation of lumped resonant circuit. For the p-i-n diode, its equivalent circuits under forward bias and reverse bias are different, which will influence the calculation of distributed elements. Under reverse bias (switch in the ON state), the admittances of two resonant circuits in Fig. 10 can be expressed as

$$Y_{in} = j\omega C_{pi} + \frac{1}{j\omega L_{pi}} + \frac{1}{j\omega(L_{ri} + L_0) + \frac{1}{j\omega C_{ri}} + \frac{1}{j\omega C_0}} \tag{18a}$$

$$Y'_{in} = \frac{1}{jZ_{pi}\tan\left(\theta_{pi}\frac{\omega}{\omega_0}\right)} + \frac{1}{Z_{ri}}\frac{Z_{ri} + jZ_L\tan\left(\theta_{ri}\frac{\omega}{\omega_0}\right)}{Z_L + jZ_{ri}\tan\left(\theta_{ri}\frac{\omega}{\omega_0}\right)} \tag{18b}$$

$$Z_L = j\omega L_0 + \frac{1}{j\omega C_0} - jZ_{ci}\cot\left(\theta_{ci}\frac{\omega}{\omega_0}\right) \tag{18c}$$

where Z_{pi}, Z_{ri}, and Z_{ci} are the characteristic impedances of TLs at f_0, and θ_{pi}, θ_{ri}, and θ_{ci} are the corresponding electric lengths at f_0.

Under forward bias (switch in the OFF state), the impedance of distributed branch with the p-i-n diode is expressed as

$$Z_{in} = Z_{ri}\frac{\left(j\omega L_0 - jZ_{ci}\cot\left(\theta_{ci}\frac{\omega}{\omega_0}\right)\right) + jZ_{ri}\tan\left(\theta_{ri}\frac{\omega}{\omega_0}\right)}{Z_{ri} + j\left(j\omega L_0 - jZ_{ci}\cot\left(\theta_{ci}\frac{\omega}{\omega_0}\right)\right)\tan\left(\theta_{ri}\frac{\omega}{\omega_0}\right)}. \tag{19}$$

By equating Z_{in} to zero, the relationship between circuit parameters and TZ of the distributed resonant circuit under forward bias $f_{\text{TZ\_DF}}$ can be obtained as

$$\omega_{TZ\_DF}L_0 - Z_{ci}\cot\left(\theta_{ci}\frac{\omega_{TZ\_DF}}{\omega_0}\right) + Z_{ri}\tan\left(\theta_{ri}\frac{\omega_{TZ\_DF}}{\omega_0}\right) = 0. \tag{20}$$

By setting (18a) equal to (18b) at the center frequency f_0, the lower band-edge frequency f_1, and the upper band-edge frequency f_2, a set of nonlinear equations with the constraint of (20) can be obtained. With the characteristic impedance Z_{pi}, Z_{ri}, Z_{ci}, and $f_{\text{TZ\_DF}}$ predefined, the parameters θ_{pi}, θ_{ri}, and θ_{ci} can be numerically solved. Note that the parameters of distributed resonant circuits are not unique due to the nonlinearity equation.

For example, with $f_1 = 3$ GHz, $f_0 = 4$ GHz, $f_2 = 5$ GHz, $C_{pi} = -0.4$ pF, $L_{pi} = 6$ nH, $L_{ri} = 0.57$ nH, $C_{ri} = 9$ pF, $L_0 = 0.4$ nH, and $C_0 = 0.78$ pF, choosing Z_{pi}, Z_{ri}, and Z_{ci} as 80, 80, and 20 Ω, respectively, θ_{pi}, θ_{ri}, and θ_{ci} can be calculated with different $f_{\text{TZ\_DF}}$. For distributed circuit 1, $f_{\text{TZ\_DF}}$ is set as 3.4 GHz, and the values of θ_{pi}, θ_{ri}, and θ_{ci} are 54.6°, 9.2°, and 53.8°, respectively; for distributed circuit 2, $f_{\text{TZ\_DF}} = 4$ GHz, $\theta_{pi} = 54.2°$, $\theta_{ri} = 15.6°$, and $\theta_{ci} = 42.8°$. Fig. 11 shows the input admittances of the lumped circuit and two distributed circuits. As illustrated in Fig. 11(a) and (b), under reverse bias, good agreement between lumped circuits and distributed circuits can be achieved within the passband while the TZs of distributed circuits will deviate from that of the lumped circuits. In Fig. 11(c), the TZs of two distributed circuits under the forward bias are exactly located at the designated position. It means that the arrangement of $f_{\text{TZ\_DF}}$ hardly affects the approximation within the passband under reverse bias.

However, there is a significant discrepancy in the input admittances under the forward bias of lumped resonant circuit and its distributed approximations. As presented in Fig. 11(c), the TZ of the lumped circuit under forward bias is around 1.7 GHz, which is far away from that of two distributed circuits. This observation can be addressed by analyzing circuits

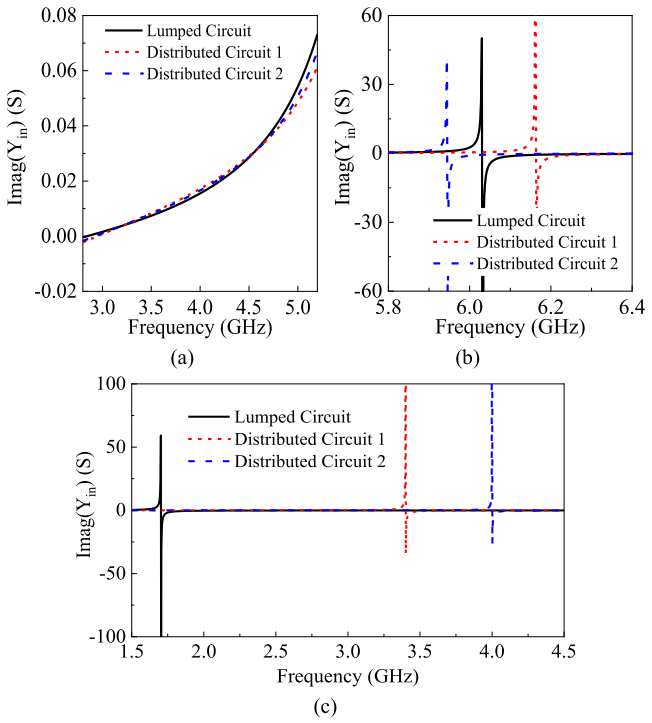

Fig. 11. Input admittances of the lumped resonant circuit and its two distributed approximation circuits under (a) reverse bias within the passband, (b) reverse bias from 5.8 to 6.4 GHz, and (c) forward bias. For distributed circuit 1, TZ under forward bias is set as 3.4 GHz. For distributed circuit 2, TZ under forward bias is set as 4 GHz.

in Fig. 10. The parameters of components in the lumped circuit are frequency-invariant, while the electric length of TLs in distributed circuits varies with the operating frequency. It will lead to the difference between lumped and distributed resonant circuits outside the frequency band bounded by f_1 and f_2.

Moreover, the nonlinear equations grouped to derive the elements of the distributed resonant circuit are attained by equating the input admittances of two circuits under reverse bias, where $f_{\mathrm{TZ\_DF}}$ is involved as the constraint. For the design of the filtering switch, it is not necessary to chase good approximations of two resonant circuits under forward bias. To achieve better isolation under forward bias, $f_{\mathrm{TZ\_DF}}$ is generally allocated within f_1 and f_2 instead of the same position with lumped resonant circuit. Therefore, the performance under the forward bias of distributed circuits, especially the location of TZ in the OFF state, will be different from that of the lumped circuits, even though the lumped circuit under reverse bias can be well approximated within the passband by the distributed circuit.

Due to the above characteristics of approximation for the resonant circuit, the frequency response of the proposed lumped switch in the OFF state is negligible in the design procedure of distributed filtering switch. Controlling the TZs of the distributed switch in the OFF state becomes an effective method to obtain high isolation in the desired frequency band. However, the options for $f_{\mathrm{TZ\_DF}}$ are limited by the parameters of the lumped resonant circuit. The electric length of the TLs in the distributed resonant circuit could be less than zero with some choices of $f_{\mathrm{TZ\_DF}}$. To avoid such a predicament in the filtering switch design, the parameters of extracted BPF network and the arrangement of TZs in the OFF state should be continuously adjusted by iterations to obtain the realizable

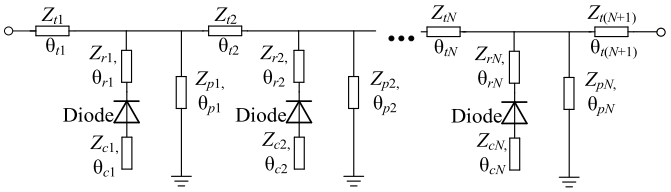

Fig. 12. Distributed circuit of the proposed filtering switch.

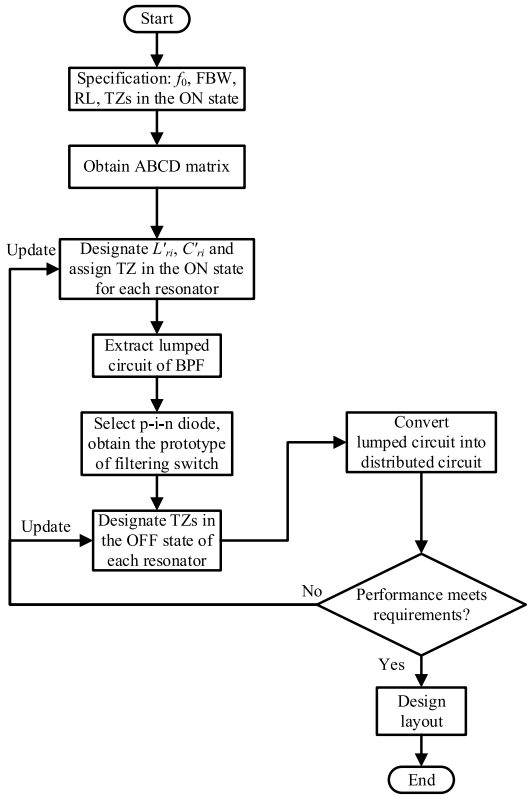

Fig. 13. Flowchart of synthesis and design procedure of the filtering switch.

parameters of the distributed circuit. Therefore, the distributed filtering switch may be obtained while the frequency response of its lumped prototype in the OFF state is totally different, as the case illustrated in Fig. 11(c).

V. Design Process of Filtering Switch

Based on the circuit approximations under wideband conditions, the lumped switch shown in Fig. 1(a) can be converted into a distributed circuit through three steps: 1) the I/O coupling inductors (L_{t1} and $L_{t(N+1)}$) and ideal transformers are approximated by TLs and shunt capacitors using (17); 2) the interresonator inductors L_{ti} ($i = 2,\ldots, N$) are replaced by their approximated distributed circuits introduced in [18]; and 3) all the shunt resonant circuits together with the shunt capacitors generated in steps 1) and 2) are approximated by the distributed circuit in Fig. 10. The topology of the distributed filtering switch is illustrated in Fig. 12.

Finally, a general synthesis and design procedure of the proposed wideband filter can be concluded by the flowchart outlined in Fig. 13. To achieve a satisfactory performance, the procedure may take several iterations of fine-tuning the L'_{ri} and C'_{ri}, modifying the assignment of TZs in the ON state and adjusting the TZs in the OFF state.

TABLE I
LUMPED ELEMENT VALUES OF FOURTH-ORDER FILTERING SWITCH

i	L_{ti} (nH)	L_{pi} (nH)	L_{ri} (nH)	C_{ri} (pF)	n_i
1	1.38	5.13	0.58	9.36	0.87
2	2.08	5.94	0.72	9.36	-
3	1.69	2.03	0.9	9.36	-
4	1.71	11.06	0.52	9.36	-
5	1.46	-	-	-	0.98

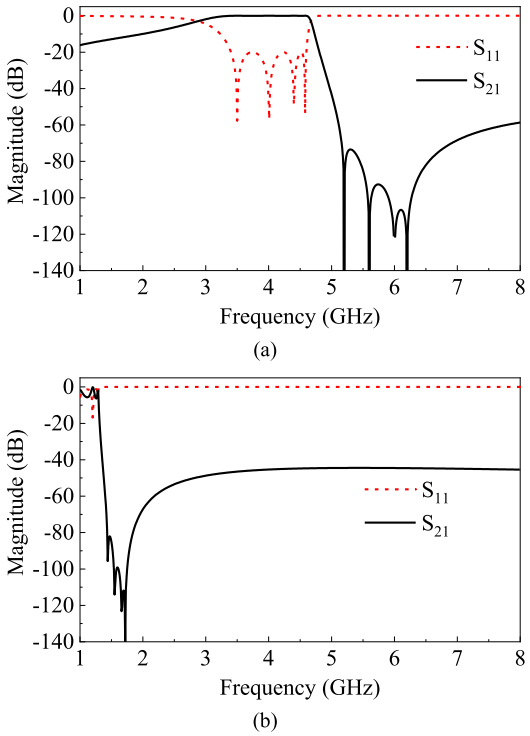

Fig. 14. *S*-parameters of lumped element circuit models of the filtering switch in (a) ON state and (b) OFF state.

TABLE II
DISTRIBUTED ELEMENT VALUES OF FOURTH-ORDER FILTERING SWITCH

i	Z_{ti} (Ω)	θ_{ti} (°) @ f_0	Z_{pi} (Ω)	θ_{pi} (°) @ f_0	Z_{ri} (Ω)	θ_{ri} (°) @ f_0	Z_{ci} (Ω)	θ_{ci} (°) @ f_0
1	61.3	29.53	100	34.89	80	12.43	20	43.12
2	80	40.82	100	44.94	80	15.72	20	47.11
3	80	31.97	100	24.98	80	17.75	30	61.45
4	80	32.4	100	60.92	80	19.11	20	24.3
5	77.7	25.28	-	-	-	-	-	-

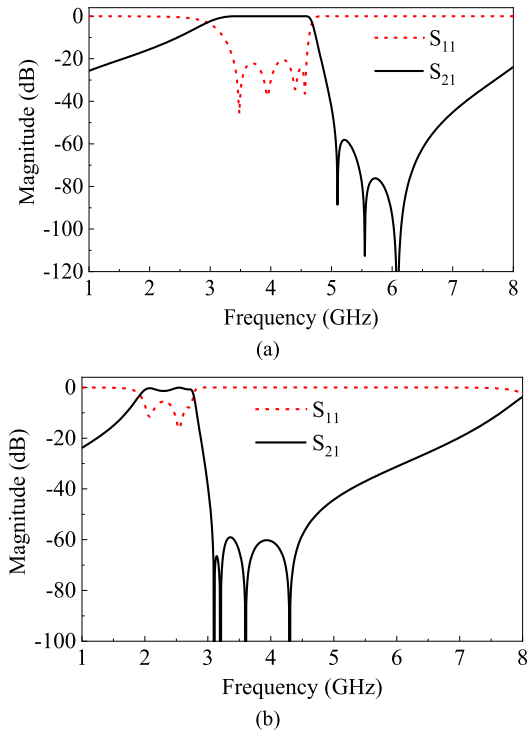

Fig. 15. *S*-parameters of the ideal distributed circuit of the filtering switch in (a) ON state and (b) OFF state.

VI. DESIGN EXAMPLES

A. Fourth-Order Filtering Switch With 30% FBW in the on State

To design a filtering switch, the BPF network should be synthesized first based on the specifications of the switch. In this example, the BPF network is designed with a center frequency of 4 GHz, FBW of 30%, fourth-order, and 20-dB in-band return loss. The TZs of four resonators are located at 6, 5.6, 5.2, and 6.2 GHz. Subsequently, the polynomial of the filter network can be synthesized according to these specifications. In this work, the MADP-030015-1314 p-i-n diode is used with a forward current of 38 mA and reverse voltage of −5 V, which exhibits $C_0 = 0.78$ pF, $L_0 = 0.4$ nH, and $R_0 = 0.49$ Ω. With all C'_{ri} as 0.72 pF, the lumped element values of the filter circuit model can be extracted. After incorporating the circuit models for the p-i-n diodes, the lumped element values of the filtering switch can be obtained and are listed in Table I. The frequency responses of the lumped filtering switch in the ON and OFF states are shown in Fig. 14.

To obtain the high isolation in the OFF state, four TZs in the OFF state are arranged at 3.6, 3.2, 3.1, and 4.3 GHz. With the proposed approximations, the parameters of the distributed circuit can be determined according to the predefined characteristic impedances, as listed in Table II. Fig. 15 illustrates the frequency responses of the ideal distributed circuit model of the filtering switch.

For the prototype of a fourth-order filtering switch, the Rogers RO4003 substrate with a dielectric constant of 2.2, loss tangent of 0.0027, and thickness of 0.813 mm, is used. Fig. 16 presents the layout of the designed fourth-order filtering switch with dimensions marked. The dc biasing circuit includes a high-impedance meander line, a 90° fan stub, and a chip resistor [19], [20]. The final dimensions are listed in Table III, and the photograph of the fabricated switch is shown in Fig. 17.

The simulated and measured results of the fourth-order filtering switch in the ON and OFF states are shown in Fig. 18(a) and (b), respectively. In the ON state, the measured return loss within the passband is greater than 15 dB. In addition, the values of measured insertion losses at the lower band-edge frequency 3.4 GHz, the center frequency 4 GHz, and the upper band-edge frequency 4.6 GHz are 1.51, 2.17, and 8.15 dB, which are 1.05, 1.62, and 4.94 dB more than the simulated results, respectively. The discrepancy of insertion

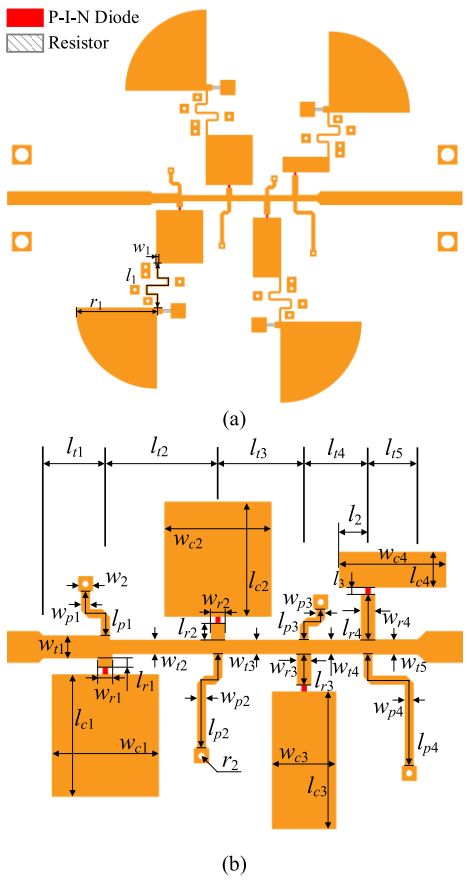

Fig. 16. (a) Layout of the fabricated fourth-order filtering switch and (b) details of the center part of (a).

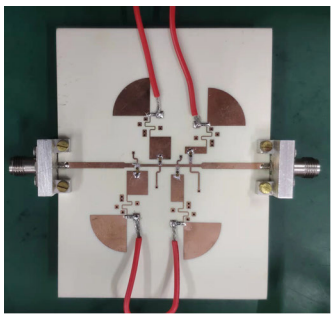

Fig. 17. Photograph of the fourth-order filtering switch.

losses within the ON-state passband at high frequencies exists, which may be caused by the losses from the p-i-n diodes and the bias circuits. In the OFF state, it can be seen that the isolation of the switch is better than 45 dB from 3.4 to 4.6 GHz (i.e., 30% FBW). The overall size of the fourth-order filtering switch (including feedlines and bias circuits) is 62.8 mm × 54.18 mm, namely, $0.84\lambda_0 \times 0.722\lambda_0$, where λ_0 denotes the guided wavelength at 4 GHz in free space.

B. Fifth-Order Filtering Switch With 50% FBW in the on State

The second example is a fifth-order filtering switch with 50% FBW in the ON state. First, the BPF network is synthesized with the specifications of the center frequency of 4 GHz, 50% FBW, fifth-order, 20-dB in-band return loss, and TZs of five resonators located at 7, 6, 6, 6, and 6.7 GHz. By designating C'_{ri} as 0.7, 0.74, 0.74, 0.7, and 0.66 pF, the lumped element values of the filter topology can be extracted.

TABLE III
FINAL DIMENSIONS OF FOURTH-ORDER SWITCH (UNIT: mm)

i	1	2	3	4	5
w_{ti}	1.27	0.75	0.75	0.75	0.8
w_{ri}	0.75	0.75	0.75	0.75	-
w_{ci}	6.39	6.39	3.8	6.39	-
w_{pi}	0.43	0.43	0.43	0.43	-
l_{ti}	3.8	6.84	5.23	3.88	3.05
l_{ri}	0.6	1	1.87	2.72	-
l_{ci}	7.25	6.8	8.16	2.05	-
l_{pi}	3.97	6.78	2.93	9.3	-
w_i	0.2	0.8	-	-	-
l_i	12.2	1.7	0.5	-	-
r_i	11.1	0.25	-	-	-

TABLE IV
LUMPED ELEMENT VALUES OF THE FIFTH-ORDER FILTERING SWITCH

i	L_{ti} (nH)	L_{pi} (nH)	L_{ri} (nH)	C_{ri} (pF)	n_i
1	1.16	15.98	0.34	6.83	0.92
2	1.71	5.19	0.55	14.43	-
3	1.57	6.12	0.55	14.43	-
4	1.61	7.24	0.61	6.83	-
5	1.7	12.44	0.45	4.29	-
6	-	-	-	-	0.9

TABLE V
DISTRIBUTED ELEMENT VALUES OF THE FIFTH-ORDER FILTERING SWITCH

i	Z_{ti} (Ω)	θ_{ti} (°) @ f_0	Z_{pi} (Ω)	θ_{pi} (°) @ f_0	Z_{ri} (Ω)	θ_{ri} (°) @ f_0	Z_{ci} (Ω)	θ_{ci} (°) @ f_0
1	65.89	23.78	100	68.12	80	7.15	30	42.65
2	70	37.84	100	47.98	80	9.44	30	63.74
3	70	34.2	100	47.97	80	7.19	20	70.62
4	70	35.41	100	47.6	80	9.18	20	59.33
5	70	37.61	100	54.73	80	7.43	30	45.07
6	56.91	25.31						

TABLE VI
FINAL DIMENSIONS OF THE FIFTH-ORDER FILTERING SWITCH (UNIT: mm)

i	1	2	3	4	5	6
w_{ti}	1.11	0.99	0.99	0.99	0.99	1.45
w_{ri}	0.75	0.75	0.75	0.75	0.75	-
w_{ci}	3.8	3.8	6.39	6.39	3.8	-
w_{pi}	0.43	0.43	0.43	0.43	0.43	-
l_{ti}	2.41	5.67	4.65	5.18	5.31	3.02
l_{ri}	1.33	1.75	0.33	0.67	1.47	-
l_{ci}	3.98	5.41	10.07	7.86	4.75	-
l_{pi}	9.07	9.11	5.48	7.19	6.86	-
w_i	0.2	0.2	0.8	-	-	-
l_i	9.8	8	0.5	1.4	-	-
r_i	10	10	0.25	-	-	-

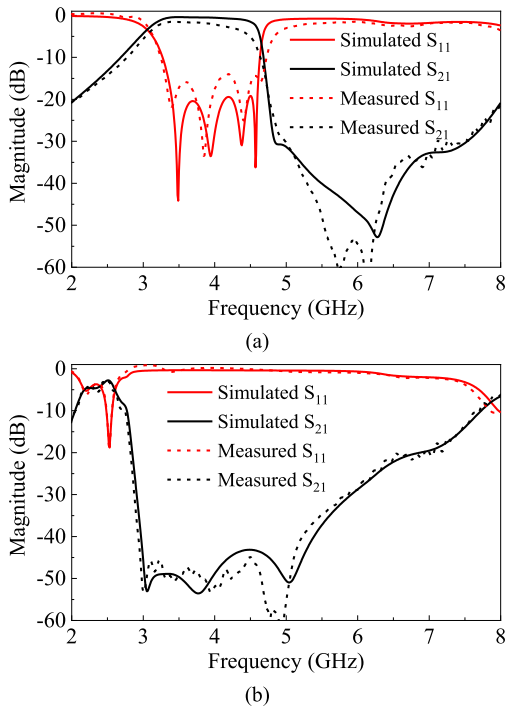

Fig. 18. Simulated and measured *S*-parameters of the prototyped fourth-order filtering switch in (a) ON state and (b) OFF state.

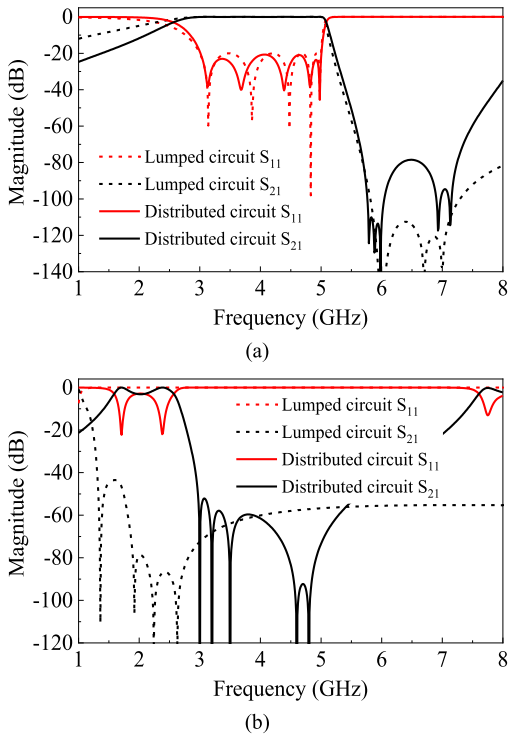

Fig. 19. *S*-parameters of lumped and distributed element circuits of the fifth order-filtering switches in (a) ON state and (b) OFF state.

After incorporating the circuit models for the p-i-n diodes, the lumped element values of the filtering switch can be obtained as listed in Table IV. By arranging TZs in the OFF state at 4.8, 3.5, 3, 3.2, and 4.6 GHz, the parameters of distributed element circuit can be derived and listed in Table V. Fig. 19

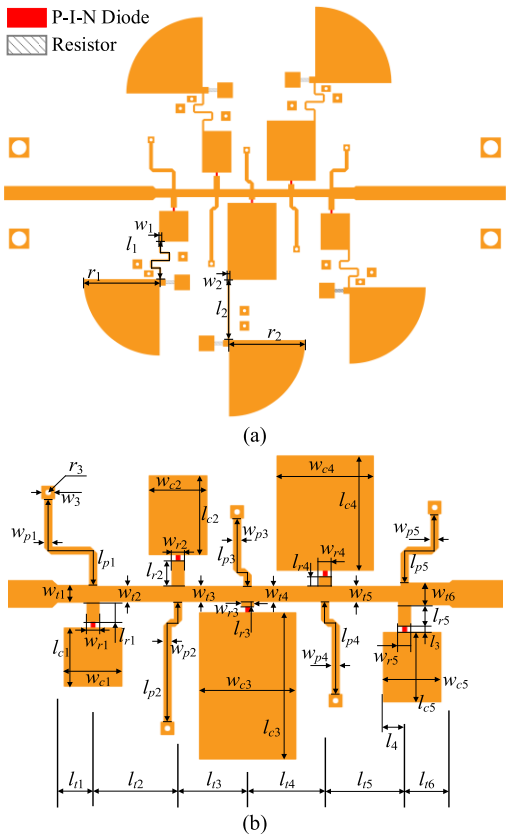

Fig. 20. (a) Layout of the fabricated fifth-order filtering switch and (b) details of the center part of (a).

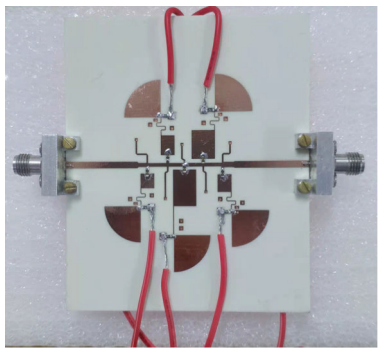

Fig. 21. Photograph of the fifth-order filtering switch.

illustrates the frequency responses of the lumped circuit and the ideal distributed circuit of the filtering switch.

Fig. 20 presents the layout of the designed fifth-order filtering switch, and the final dimensions are listed in Table VI. The photograph of the fabricated switch is shown in Fig. 21. The simulated and measured results of the fifth-order switch are shown in Fig. 22. In the ON state, as seen in Fig. 22(a), the measured return loss within the passband is greater than 14 dB. In addition, the measured insertion losses at 3, 4, and 5 GHz are 0.97, 1.45, and 7.27 dB, respectively. Similar to the fourth-order filtering switch, the larger discrepancy of insertion losses between simulated and measured results can be observed at higher frequencies in Fig. 22(a). In the OFF state, the isolation of the switch is better than 30 dB from 3 to 5 GHz (i.e., 50% FBW), as illustrated in Fig. 22(b). The overall

TABLE VII
PERFORMANCE COMPARISONS BETWEEN THE PROPOSED FILTERING SWITCHES AND REPORTED WORKS

	Type	Technology	Frequency (GHz)	FBW	ON state IL(dB)	TZ	OFF state Isolation(dB)
[2]	SPST	On-chip + FET	24.2-36.3	40.8%	1.75-2.25	No	>58
[8]	SPDT	On-chip + FET	40	8%	>3.1	Yes	>30
[10]	SPDT	DR + P-I-N Diode	1.861	1.16%	0.51#	No	>32
[11]	SPQT	CR + P-I-N Diode	2.37	2.9%	0.93*	Yes	>25.8
[13]	SPST	PCB + P-I-N Diode	1.5	5%	3.9#	No	>34
[14]	SPDT	PCB + P-I-N Diode	0.612-1.088	19.5%	2.3-2.8	No	>41.4
[15]	SPDT	PCB + P-I-N Diode	0.89/1.82	8.3%/ 9.6%	2.06*/2.05*	Yes	>42.2
This work	SPST	PCB + P-I-N Diode	**3.4-4.6**	**30%**	1.51*	Yes	>45
			3-5	**50%**	0.97*	Yes	>30

Notes: DR means dielectric resonator, CR means coaxial resonator, # denotes the insertion loss at center frequency, * denotes the minimun insertion loss within passband.

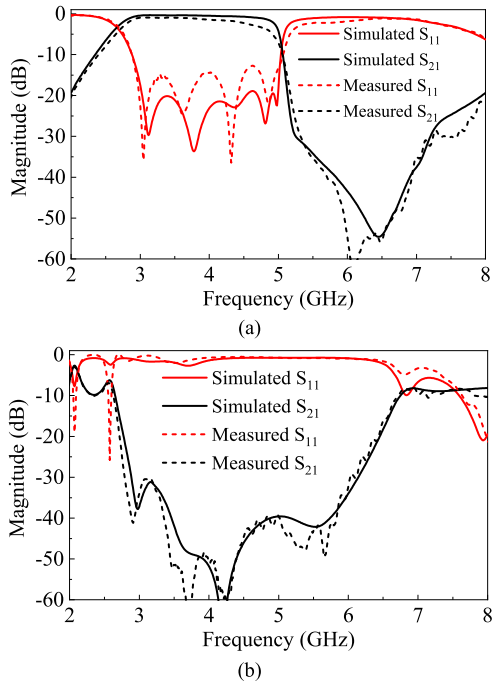

Fig. 22. Simulated and measured *S*-parameters of prototyped fifth-order filtering switch in (a) ON state and (b) OFF state.

size of the fifth-order filtering switch (including feedlines and bias circuits) is 66.24 mm × 53.9 mm ($0.88\lambda_0 \times 0.719\lambda_0$). For further illustration, a table of comparisons between the reported filtering switches and the proposed works is given in Table VII.

VII. CONCLUSION

In this article, a novel wideband filtering switch is proposed together with the direct synthesis and design processes. By incorporating the circuit model of the p-i-n diodes in the resonators of the filtering network, the circuit models of the filtering switch operating in the ON states can be synthesized according to the specifications. Moreover, the ideal transformers are introduced to designate the capacitances and inductances of each resonator with proper values directly, which ensures all elements of the filtering switch are feasible. Then, the lumped filtering switch embedding p-i-n diodes will be transformed into distributed circuits in a wide frequency range. Due to the frequency-variant characteristic of TLs, the TZs in the OFF state can be adjusted to a suitable position after converting the lumped element circuit to a distributed element circuit. Therefore, high isolation in the desired frequency band can be obtained by controlling the TZs of the distributed switch in the OFF state. To validate the proposed filtering switch as well as the synthesis and design process, two filtering switches with FBWs of 30% and 50% are designed and measured. Good agreement between the simulated and measured results is obtained.

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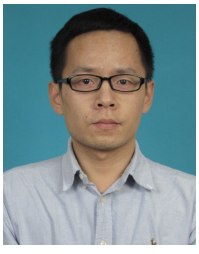

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